Program Structure for Third Year UG Technology (EX)
Semester-V - Credit Scheme

Course Code	Course Name	Teaching Scheme (Hrs.) TH – P – TUT	Total (Hrs.)	Credits Assigned TH – P – TUT	Total Credits	Course Category
EXC501	Digital Communication	3– 0 – 0	03	3 – 0 – 0	03	PC
EXC502	Digital VLSI Design	3– 0 – 0	03	3 – 0 – 0	03	PC
EXC503	Discrete Time Signal Processing	3– 0 – 0	03	3 – 0 – 0	03	PC
EXC504	Random Signal Analysis	3 – 0 – 0	03	3 – 0 – 0	03	PC
EXDLC505	Department Level Elective Course - I	3 – 0 – 0	03	3 – 0 – 0	03	DLE
EXL501	Digital Communication Laboratory	0 – 2 – 0	02	0 – 1 – 0	01	PC
EXL502	Digital VLSI Design Laboratory	0 – 2 – 0	02	0 – 1 – 0	01	PC
EXL503	Discrete Time Signal Processing Laboratory	0 – 2 – 0	02	0 – 1 – 0	01	PC
EXDLL505	Department Level Elective Course Laboratory- I	0 – 2 – 0	02	0 – 1 – 0	01	DLE
EXL506	Business Communication & Ethics Laboratory	0 – 4** – 0	04	0 – 2– 0	02	BS
EXPR53	Project Based Learning – Minor Project Lab - I	0 – 2 – 0	02	0 – 1 – 0	01	PBL
EXXS57	Skill Based Learning -VII	0 – 2*- 0	02	0 – 1 – 0	01	SAT
EXXT58	Technology Based Learning - VIII	0 – 2*- 0	02	0 – 1 – 0	01	SAT
Total		**15– 18 – 00**	**33**	**15 – 09 – 00**	**24**	

	Course Code	Course Title and Group
Department Level Elective Course - I	EXDLC5051	Group A: Data Compression & Encryption
	EXDLC5052	Group B: Sensor Technology
	EXDLC5053	Group C: Microelectronics Devices and Circuit
	EXDLC5054	Group D: Data Structure and Algorithms

***SAT Hours are under Practical head but can be taken as Theory or Practical or both as per the need.**
****2 Hours class wise and 2 hours batchwise**
 # 1 Credit = 40 – 45 hours of Internship (Refer Internship document)

PBL - Minor Project Lab I and II:
- Students can form groups with minimum 2 (Two) and not more than 4 (Four)
- Faculty Load : 1 hour per week per four groups

Program Structure for Third Year UG

Technology (EX)
Semester-V- Examination Scheme

Course Code	Course Name	Examination Scheme								
		Marks								
		CA				ESE	TW	O	P	Total
		T1	T2	Average (T1&T2)	IA					
EXC501	Digital Communication	30	30	30	10	60	-	-	-	100
EXC502	Digital VLSI Design	30	30	30	10	60	-	-	-	100
EXC503	Discrete Time Signal Processing	30	30	30	10	60	-	-	-	100
EXC504	Random Signal Analysis	30	30	30	10	60	-	-	-	100
EXDLC505	Department Level Elective Course - I	30	30	30	10	60	-	-	-	100
EXL501	Digital Communication Laboratory	-	-	-	-	-	25	-	25	50
EXL502	Digital VLSI Design Laboratory	-	-	-	-	-	25	-	25	50
EXL503	Discrete Time Signal Processing Laboratory	-	-	-	-	-	25	-	-	25
EXDLL505	Department Level Elective Course Laboratory- I	-	-	-	-	-	25	-	-	25
EXL506	Business Communication & Ethics	-	-	-	-	-	25	25	-	50
EXPR53	Project Based Learning – Minor Project Lab – I	-	-	-	-	-	25	-	25	50
EXXS57	Skill Based Learning –VII	-	-	-	-	-	25	-	-	25
EXXT58	Technology Based Learning -VIII	-	-	-	-	-	25	-	-	25
Total		150	150	**150**	**50**	**300**	**200**	**25**	**75**	**800**

Program Structure for Third Year UG Technology (EX)
Semester-V- Examination Scheme

Course Code	Course Name	Examination Scheme								
		Marks								
		CA				ESE	TW	O	P	Total
		T1	T2	Average	IA					

				(T1&T2)						
EXC501	Digital Communication	30	30	30	10	60	-	-	-	100
EXC502	Digital VLSI Design	30	30	30	10	60	-	-	-	100
EXC503	Discrete Time Signal Processing	30	30	30	10	60	-	-	-	100
EXC504	Random Signal Analysis	30	30	30	10	60	-	-	-	100
EXDLC505	Department Level Elective Course - I	30	30	30	10	60	-	-	-	100
EXL501	Digital Communication Laboratory	-	-	-	-	-	25	-	25	50
EXL502	Digital VLSI Design Laboratory	-	-	-	-	-	25	-	25	50
EXL503	Discrete Time Signal Processing Laboratory	-	-	-	-	-	25	-	-	25
EXDLL505	Department Level Elective Course Laboratory- I	-	-	-	-	-	25	-	-	25
EXL506	Business Communication & Ethics	-	-	-	-	-	25	25	-	50
EXPR53	Project Based Learning – Minor Project Lab – I	-	-	-	-	-	25	-	25	50
EXXS57	Skill Based Learning –VII	-	-	-	-	-	25	-	-	25
EXXT58	Technology Based Learning -VIII	-	-	-	-	-	25	-	-	25
Total		150	150	**150**	**50**	**300**	**200**	**25**	**75**	**800**

Program Structure for Third Year UG Technology (EX)

Semester-V- Examination Scheme

Course Code	**Course Name**	**Examination Scheme**								
		Marks								
		CA				**ESE**	**TW**	**O**	**P**	**Total**
		T1	T2	**Average (T1&T2)**	**IA**					
EXC501	Digital Communication	30	30	30	10	60	-	-	-	100
EXC502	Digital VLSI Design	30	30	30	10	60	-	-	-	100
EXC503	Discrete Time Signal Processing	30	30	30	10	60	-	-	-	100
EXC504	Random Signal Analysis	30	30	30	10	60	-	-	-	100
EXDLC505	Department Level Elective Course - I	30	30	30	10	60	-	-	-	100
EXL501	Digital Communication Laboratory	-	-	-	-	-	25	-	25	50
EXL502	Digital VLSI Design Laboratory	-	-	-	-	-	25	-	25	50

EXL503	Discrete Time Signal Processing Laboratory	-	-	-	-	-	25	-	-	25
EXDLL505	Department Level Elective Course Laboratory- I	-	-	-	-	-	25	-	-	25
EXL506	Business Communication & Ethics	-	-	-	-	-	25	25	-	50
EXPR53	Project Based Learning – Minor Project Lab – I	-	-	-	-	-	25	-	25	50
EXXS57	Skill Based Learning –VII	-	-	-	-	-	25	-	-	25
EXXT58	Technology Based Learning -VIII	-	-	-	-	-	25	-	-	25
Total		150	150	**150**	**50**	**300**	**200**	**25**	**75**	**800**

Course Code	**Course Name**	**Credits (TH+P+TUT)**
EXC501	**Digital Communication**	**3+0+0**

Prerequisite:	1. Applications of Mathematics in Engineering-II 2. Signals and Systems 3. Principles of Communication Engineering
Course Objectives:	To describe the basics of information theory and source coding To illustrate various error control codes To describe baseband system To learn different digital modulation and demodulation techniques
Course Outcomes:	Apply the concepts of information theory in source coding Apply different error control systems and various error detection codes Analyse different error correction codes Compare various baseband transmission methods for digital signals Evaluate the performance of optimum baseband detection in the presence of white noise Compare the performances of different digital modulation techniques

Module No. & Name	**Sub Topics**	**CO Mapped**	**Hrs/ Sub Topic**	**Total Hrs/ Module**
. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
. Information Theory and Source Codes	Block diagram of digital communication system, Information content of a source symbol, Source entropy, Average information rate, AWGN channel, and Shannon-Hartley channel capacity theorem	1	03	05
	Introduction of source code, Huffman code,		02	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Shannon-Fano code			
. Error Control System and Error Detection Codes	Introduction of error control system, Automatic Retransmission Query (ARQ) system, Types of ARQ systems and comparison, Forward error correction (FEC) system. Comparison between FEC and ARQ	2	01	03
	Error detection codes: Vertical Redundancy Check (VRC) code, Longitudinal Redundancy Check (VRC) code, Cyclic Redundancy Check (CRC) code and Checksum code		02	
3. Error Correction Codes	Linear block code: Code generation, calculation of minimum Hamming distance, error detection capability, error correction capability, implementation of encoder, error detection, syndrome table, error correction and implementation of decoder	3	03	10
	Cyclic code: Code generation, calculation of minimum Hamming distance, error detection capability, error correction capability, implementation of encoder, error detection, syndrome table, error correction and implementation of decoder		03	
	Convolutional code: Generation, path responses, encoder, state transition table, state diagram, tree diagram, trellis diagram, decoding using Viterbi's algorithm		04	
4. Baseband Transmission	Block diagram of baseband transmitter-receiver system, Line codes (RZ and NRZ Uni Polar formats, RZ and NRZ Polar formats, NRZ Bipolar format (AMI format), NRZ Manchester format, and Quaternary Polar format). Comparison of line codes with respect to bandwidth, power requirement, synchronization capability, DC level, polarity inversion error and complexity. Power spectral density and spectrum of NRZ Unipolar and Polar formats	4	03	05
	Inter Symbol Interference (ISI), Inter Channel Interference (ICI). Nyquist criterion for distortion less baseband binary transmission, Nyquist bandwidth and		02	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	practical bandwidth			
. Optimum Detection of Baseband Signal	Matched filter, Output SNR, Transfer function, Impulse response and Error probability. Integrate and dump receiver, Correlator receiver	5	04	04
6. Digital Modulations	Generation, Detection, Error probability (using signal space representation and Euclidean distance), Bandwidth (using PSD and spectrum except for MSK) and applications of the following modulations: Binary ASK, Binary PSK, Quadrature PSK, Off-Set QPSK, M-ary PSK, Binary FSK, M-ary FSK, 16-ary QASK and MSK	6	12	12
. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. Principles of Communication Systems, Third Edition, H.Taub, D.Schlling and G.Saha, Tata Mc-Graw Hill, New Delhi, 2012 2. Modern Digital and Analog Communication Systems, Fourth Edition, Lathi BP and Ding Z, Oxford University Press, 2009 3. Digital Communication System, Fourth Edition, Haykin Simon John Wiley and Sons, New Delhi 2014 4. Digital Communications, Fourth Edition, John G. Proakis, McGraw-Hill
Reference Books	1. Digital Communication: Fundamentals and applications, Second Edition 2. Sklar B, and Ray P. K. Pearson, Dorling Kindersley (India), Delhi, 2009 3. Analog and Digital Communication, First Edition, T L Singal, Tata Mc-Graw Hill, New Delhi, 2012 4. Digital Communication, First Edition, P Ramakrishna Rao, Tata Mc-Graw Hill, New Delhi, 2011
Useful Links:	
1. https://nptel.ac.in/courses/117/101/117101051/ 2. https://nptel.ac.in/courses/117/105/117105077/ 3. https://nptel.ac.in/courses/108/101/108101113/ 4. https://nptel.ac.in/courses/108/102/108102096/ 5. https://nptel.ac.in/courses/108/102/108102120/	

Continuous Assessment (CA):
The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks):
Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment.

Internal Assessment(IA):
Marks will be awarded based on the rubrics designed.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Course Name	Credits (TH+P+TUT)
EXC502	**Digital VLSI Design**	**3+0+0**
Prerequisite:	Electronics Devices & Circuits Digital Logic Design	
Course Objectives:	To introduce process flow of VLSI Design To understand MOSFET operation from VLSI design perspective To learn VLSI design performance metric and trade-offs To design, implement and verify combinational and sequential logic circuits using various MOS design styles To provide an exposure to RTL design	
Course Outcomes:	1. Explain various tools and processes used in VLSI Design 2. Derive expressions for performance parameters of basic building blocks like CMOS inverter 3. Design and realize various combinational and sequential circuits for given specifications 4. Explain working of building blocks of semiconductor memory 5. Illustrate various data path circuits and the issues related to the design of the VLSI system 6. Design digital systems using RTL design technique	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
. Review of MOSFET operation and Fabrication	MOSFET structure and operation, IV characteristics, MOSFET Capacitances, MOSFET scaling	1	02	05

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Overview of VLSI Design Flow, Fabrication process flow of NMOS and CMOS, Lambda based design rules, Stick diagram and mask layout		03	
. **Combinational CMOS Logic Circuits**	CMOS inverter operation, Voltage Transfer characteristics (VTC), Noise Margins, Propagation Delay, Power Dissipation, Design of CMOS Inverter, Layout of CMOS Inverter	2	03	06
	Realization of CMOS NAND gate, NOR gate, Complex CMOS Logic Circuits, Layout of CMOS NAND, NOR and complex CMOS circuits		03	
. **MOS Design Logic Styles**	Static CMOS, Pass Transistor Logic, Transmission Gate, Pseudo NMOS, Dynamic CMOS Logic, Domino Logic, NORA, Zipper, C^2MOS	3	04	08
	Combinational circuit design: MUX, Decoder using above design styles ,1-bit full adder Concepts of Setup time, Hold time, clocked CMOS SR Latch, CMOS JK Latch, MS –JK Flip Flop, Edge triggered D-Flip Flop, Realization of Shift Register using design styles		04	
. **Semiconductor Memories**	ROM array, 6T-SRAM (operation, design strategy, leakage currents, sense amplifier), layout of SRAM	4	04	07
	Operation of 1T and 3T DRAM Cell, NAND and NOR flash memory		03	
. **Data path and system design issues**	Ripple carry adder, CLA adder, carry save adder, carry select adder, carry skip adder, Array Multiplier, Barrel shifter	5	03	09
	On chip clock generation and distribution, Interconnect delay model, interconnect scaling and crosstalk		02	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Design for testability: Fault Types and models, Controllability and observability, Ad hoc testable design techniques, Scan based techniques, Built-in-self-test, Current monitoring test		04	
6. RTL Design	High Level state machines, RTL design process RTL design of Soda dispenser machine, Laser Based Distance Measurer, FIR Filter	6	04	04
. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. CMOS Digital Integrated Circuits Analysis and Design, Third edition, Sung-Mo Kang and Yusuf Leblebici, McGraw Hill, 2012 2. Digital Integrated Circuits: A Design Perspective, Second edition, Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Pearson Education, 2013 3. Digital Design with RTL design, VHDL and VERILOG, Second edition, Frank Vahid, John Wiley and Sons Publisher, 2010
Reference Books	1. VLSI Design: A Circuits and Systems Perspective, Third Edition, Neil H. E. Weste, David Harris and Ayan Banerjee, Pearson Education, 2012 2. Introduction to VLSI Circuits and Systems, Student Edition, John P. Uyemura, Wiley, 2013 3. CMOS Circuit Design, Layout and Simulation, Second Edition, R. Jacob Baker, Willey, 2002
Useful Links:	
1. https://nptel.ac.in/noc/courses/noc19/SEM1/noc19-ee25/ 2. https://nptel.ac.in/courses/108/103/108103108/ 3. http://cmosedu.com/	

Continuous Assessment (CA):
The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks): Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment. **Internal Assessment(IA):** Marks will be awarded based on the rubrics designed.
End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	**Course Name**	**Credits (TH+P+TUT)**
EXC503	**Discrete Time Signal Processing**	**3+0+0**
Prerequisite:	Signals & Systems	
Course Objectives:	To develop a thorough understanding of Discrete Fourier transform and its use in frequency domain filter designing To design and realize IIR filters and FIR filters, gain an appreciation for the trade-offs necessary in the filter design and to evaluate the effects of finite word lengths on the filters. To introduce applications of digital signal processing in the field of biomedical and speech signal processing	
Course Outcomes:	Identify different types of filters based on pass band of given transfer function Illustrate the concepts of Discrete Fourier transform, Fast Fourier transform and apply in system analysis Design digital IIR and FIR filters to satisfy the given specifications and evaluate the frequency response Apply Digital FIR and IIR filter to realize structures Interpret Finite word length Effect in Digital filter Apply signal processing concepts, algorithms in applications related to the field of biomedical and speech signal processing	

Module No. & Name	**Sub Topics**	**CO Mapped**	**Hrs/ Sub Topic**	**Total Hrs/ Module**
. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
. Transform Analysis of Linear Time Invariant System	LTI systems as frequency-selective filters like low pass, high pass, band pass, Notch, comb, all-Pass filters	1	03	05
	Invertibility of LTI systems, minimum-phase, maximum-phase, mixed-phase system		02	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. The Discrete Fourier Transform and Efficient Computation	Relation between DTFT and DFT, Definition and Properties of Discrete Fourier transform (DFT), Inverse DFT, Circular convolution of sequences using DFT and IDFT	2	04	10
	Linear filtering Technique based on DFT: Evaluation of Linear filtering using DFT, Linear filtering of long data sequences: overlap add and overlap save method		02	
	Fast Fourier Transform: Radix-2 Decimation in time and Decimation in frequency FFT algorithm and its Inverse, Introduction to Composite -Radix Fast Fourier Transform (FFT)		04	
. Design of Digital Filters and Implementation	Concepts of Infinite Impulse Response (IIR) filter, Mapping of S-plane to Z-plane, Design of Infinite Impulse Response (IIR) filters using Impulse Invariant Method and Bilinear transformation Method from analog filter with examples, Design of Digital Low pass and high pass Butterworth and Chebyshev-I filter from analog filter with examples	3	06	10
	2 Concepts of Finite Impulse Response (FIR) filter, Symmetric and Anti-symmetric FIR filter, Design Techniques of FIR filter using various window: Rectangular window, Hamming window, Gibb's phenomenon, Comparison of IIR and FIR filter		04	
. Digital filter structure	Realization structures for FIR systems: Cascade form, Frequency sampling structure, Lattice structure, Computational complexities for N length filter	4	03	05
	Realization structures for IIR systems: Cascade form and parallel form structures, Lattice Ladder structure, Computational complexities for N order filter	5	02	
. Finite word length Effect in Digital filter	Quantization Noise, Truncation and Rounding, Effect due to Truncation and Rounding, Coefficient quantization error	5	02	04

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Dead band, Zero input Limit cycle oscillations and Overflow Limit cycle oscillations		02	
. Applications of Digital Signal Processing	Voice Processing, Digital Representation of speech signal, Short Time Spectral Analysis of Speech signal, channel Vocoder, Sub-band Coding, Voice privacy system.	6	03	05
	Applications of DSP for ECG signal analysis		01	
	Applications of DSP for Dual Tone Multi-Frequency Signal Detection		01	
. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. Proakis J., Manolakis D., "*Digital Signal Processing*", 4th Edition, Pearson Education 2. Emmanuel C. Ifeachor, Barrie W. Jervis," Digital Signal Processing", A Practical Approach", Pearson Education 3. A Nagoor Kani "Digital Signal Processing", 2nd Edition. Tata Mc Graw Hill Education Private Limited
Reference Books	Sanjit K. Mitra, "Digital Signal Processing – A Computer Based Approach", 4th Edition McGraw Hill Education (India) Private Limited, 2013 Oppenheim A., Schafer R., Buck J., "Discrete Time Signal Processing", 2nd Edition, Pearson Education, 3rd Edition, 2010 L. R. Rabiner and B. Gold, "Theory and Applications of Digital Signal Processing", PrenticeHall of India, 2006 S Salivahan, C Gnanapriya, "Digital Signal Processing", Mc Graw Hill Education (India) limited, 4th Edition, 2015 Monson H Hayes, "Digital Signal Processing", Schaum's Outline Series, 2nd Edition, 2011 Rangaraj M. Rangayyan, "Biomedical Signal Analysis- A Case Study Approach", Wiley 2002
seful Links:	
1. Course: Digital Signal Processing By Prof. S.C Dutta Roy, IIT Delhi http://www.nptelvideos.in/2012/12/digital-signal-processing.html 2. Course: Digital Signal Processing By Prof. V. M. Gadre , IIT	

Bombay https://nptel.ac.in/courses/108/101/108101174/

3. Course: Digital Signal Processing By Prof. T. K. Basu , IIT Kharagpur https://nptel.ac.in/courses/108/105/108105055/

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks):

Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment.

Internal Assessment(IA):

Marks will be awarded based on the rubrics designed.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Course Name	Credits (TH+P+TUT)
EXC504	**Random Signal Analysis**	**3+0+0**
Prerequisite:	Applications of Mathematics in Engineering-II Signals and Systems	
Course Objectives:	To strengthen the foundations of probability To teach continuous and discrete random variables To explain statistical behaviour of one dimensional and two-dimensional random variables To describe the concept of random process which is essential for random signals and systems encountered in Communications To develop problem solving skills and explain how to make the transition from a real-world problem to a probabilistic model	
Course Outcomes:	Apply theory of probability in identifying and solving relevant problems Elucidate and Differentiate Random Variables and Vector through the use of cumulative distribution function (CDF), Probability density function (PDF), probability Mass function (PMF) as well as Joint, Marginal and Conditional CDF, PDF and PMF. Articulate expectation and variance of random variables using special distributions Apply concepts to multiple random variables and investigate significance of Central Limit Theorem	

	Illustrate and specify Random processes and determine whether given process is stationary or wide sense stationary Describe basic concept of Markov chain related to real world applications

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
. Basic Concept in Probability	Definitions of Probability, Joint, Conditional and Total Probability, Bayes' Theorem, Independence of events.	1	03	04
	Binary symmetric communication channel analysis using Bayes' Theorem.		01	
. Introduction to Random variables	Continuous & Discrete Random Variables, Probability Density Function, Probability Distribution Function, and Probability Mass Function, Properties of PDF and CDF.	2	04	08
	Special distributions- Binomial, Poisson, Uniform, Gaussian and Rayleigh Distributions and its Mean, variance and moments of random variables		04	
. Operations on One Random Variable	Function of a random variable and their distribution and density functions	3	04	08
	Expectation, Variance, Moments, and Characteristic function of random variable.		04	
. Multiple random variables	Pairs of random variables, Joint CDF and Joint PDF	4	02	08
	One function of two random variables, Joint moments, covariance and correlation independent, uncorrelated and orthogonal random variables		05	
	4.3 Central limit theorem and its significance.		01	
. Random Processes	Definitions, statistics of stochastic processes, n^{th} order distribution, second-order properties: mean and autocorrelation, SSS, WSS	5	04	06
	Mean and Correlation Ergodic Processes, Power Spectral Density Functions and its properties		02	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. Markov Chains	6.1 Markov process, Discrete Markov chains	6	01	05
	The n–step Transition Probabilities, Chapman-Kolmogorov equations (for discrete Markov Chain), Steady State probabilities, Classification of States of Markov Chain		04	
. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. T. Veerarajan, "Probability, Statistics and Random Process", Tata McGraw Hill Education, Third Edition (2018). 2. Athanasios Papoulis and S. Unnikrishnan Pillai, "Probability, Random Variables, and Stochastic Processes", Tata McGraw Hill Education 3. Henry Stark & John Woods, "Probability, Statistics, and Random Processes for Engineers,4th Edition, Pearson Education, 2012
Reference Books	1. Scott Miller and Donald Childers, "Probability and Random Processes with Applications to Signal Processing and Communications", Elsevier Publication Hwei Hsu, "Theory and Problems of Probability, Random Variables, and Random Processes", Schaum's Outline Series, McGraw Hill, 1997 2. P. Ramesh Babu, "Probability Theory and Random Process", Tata McGraw Hill Education 3. Alberto Leon Garcia, "Probability and Random Processes for Electrical Engineering", second edition, Pearson education 4. Ronald Walpole, et. al., "Probability and Statistics for Engineers and Scientists", 8th edition, Pearson Education 5. P. Kousalya, "Probability, Statistics, and Random Processes", Pearson Education
Useful Links:	
1. Introduction to probability and Statistics, Prof. G. Srinivasan (IIT Madras): https://onlinecourses.nptel.ac.in/noc21_ma01/preview 2. Probability and Probability Distributions By Dr. P.Nagesh:\ https://onlinecourses.swayam2.ac.in/cec21_ma02/preview	

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks):
Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment.

Internal Assessment(IA):
Marks will be awarded based on the rubrics designed.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Department Level Elective Course - I	Credits (TH+P+TUT)
EXDLC5051	**Data Compression and Encryption**	**3+0+0**
Prerequisite:	Applications of Mathematics in Engineering-I	
Course Objectives:	1. To understand data compression methods for text, images, video and audio. 2. To study different source coding techniques of data compression. . To understand the concepts of cryptography and different algorithms to provide system security 4. To learn to apply different cryptographic techniques	
Course Outcomes:	1. Apply different compression techniques on text 2. Explain different data compression methods and standards 3. Explain symmetric and asymmetric cryptography techniques and standards . Apply different ciphers and number theory concepts and algorithms to solve the cryptographic problems 5. Describe methods that provide integrity, confidentiality and authentication . Describe system security facilities designed to protect the system from security threats	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
1. Introduction to Data Compression	1 Data compression, modelling and coding, Lossless and Lossy Compression, Arithmetic Coding – Decoding, Dictionary Based Compression, Sliding Window Compression: LZ-77, LZ-78, LZW	1	05	08
	2 Image Compression: DCT, JPEG, JPEG – LS, Differential Lossless Compression, DPCM, JPEG – 2000 Standards	2	03	
. Video and Audio Compression	1 Video compression: Motion compensation, temporal and spatial prediction, MPEG-4, H.264 encoder and decoder.	2	03	06
	2 Sound, Digital Audio, μ-Law and A-Law Companding, MPEG –4 Audio Layer, Advanced Audio Coding (AAC) standard		03	
3. Data Security	1 Security Goals, Cryptographic Attacks and Techniques	3	02	09
	2 Symmetric Key: Substitution Cipher, Transposition Cipher , Stream and Block Cipher		05	
	3 DES, double DES and triple DES, AES		02	
. Number Theory	1 Prime Numbers, Fermat's and Euler's Theorem	4	02	04
	2 Chinese Remainder Theorem		02	
. Asymmetric Key Cryptography	1 Principles of Public Key Crypto System, RSA, Key Management, Deffie-Hellman Key Exchange	5	04	08
	2 Message Integrity, Message Authentication and Hash Functions, SHA, HMAC, Digital Signature Standards		04	
6. System Security	1 Intrusion Detection System, Secure Electronic Transactions	6	02	04
	2 Firewall Design, Digital Immune systems, Biometric Authentication, Ethical Hacking		02	
. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. Khalid Sayood, 3rd Edition, Introduction to Data Compression, Morgan Kauffman 2. Mark Nelson, Jean-Loup Gailly, The Data Compression Book, 2nd

	edition, BPB Publications 3. William Stallings, Cryptography and Network Security Principles and Practices 5th Edition, Pearson Education. 4. Behrouz A. Forouzan, Cryptography and Network Security, Tata McGraw-Hill.
Reference Books	1. David Salomon, Data Compression: The Complete Reference, Springer 2. Matt Bishop, Computer Security Art and Science, Addison-Wesley 3. Bernard Menesez, Network Security and Cryptography, Delmar Cengage Learning, 7th Edition

Useful Links:

1. http://www.nptelvideos.com/video.php?id=989
2. https://www.coursera.org/lecture/algorithms-part2/introduction-to-data-compression-OtmHU
3. https://nptel.ac.in/courses/106102064/19
4. 4.https://www.coursera.org/learn/crypto?_escaped_fragment_=&trk=profile_certification_title
5. https://onlinecourses.nptel.ac.in/noc21_cs16/preview/

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks):

Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment.

Internal Assessment(IA):

Marks will be awarded based on the rubrics designed.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Department Level Elective Course - I	Credits (TH+P+TUT)
EXDLC5052	**Sensor Technology**	**3+0+0**
Prerequisite:	1. Electronics Devices and Circuits 2. Linear Integrated Circuits	
Course Objectives:	1. To explain basics of sensing techniques and parameters 2. To familiarize about MEMS sensors and Actuators 3. To provide exposure to wireless sensing technologies using sensors and	

	signal conditioning. 4. To provide insight into various sensor applications
Course Outcomes:	1. Describe the transduction principle of various sensors. 2. Select sensors suitable for required application 3. Analyse wireless sensing techniques 4. Identify signal conditioning method for particular application 5. Design the data acquisition system 6. Implement applications using various sensor technologies

Module No.	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
1. Introduction	1 Classification of Sensors: The sensors are classified with criteria like primary physical quantity to be sensed, transduction principle, material and technology used and application	1	01	03
	2 Criteria to choose a Sensor: Accuracy, Precision, Resolution, Environmental condition, Range, Calibration, and Cost		01	
	3 Smart Sensors: Low-power, Self – diagnostic and Self- calibration		01	
2. Types of Sensors	1 Temperature Sensors: RTD, Thermocouple and Thermistors sensor	2	02	09
	2 Proximity Sensors: Inductive (LVDT), Capacitive, Photoelectric and Ultrasonic sensors		02	
	3 Chemical Sensors: Gas, Smoke, Conductivity and pH sensor		02	
	4 Other Sensors: Optical, Infrared (IR), Sound, Motion, Pressure, Level, Moisture, Humidity, Laser, UV sensors, Ac, IR and Segmented Sensors.		03	
3. MEMS Sensors and Actuators	1 MEMS Sensors: General design methodology, techniques for sensing, Pressure sensor , Acceleration sensor, Accelerometers, Angular Rate sensor and Gyroscopes, Micro machined microphones, Chemical sensors	2	03	06

Module No.	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	2 MEMS Actuators: Techniques for actuation, Digital Micro mirror Device, Micro Machined Valves, Microfluid Devices, IEEE P1451 standard		03	
4. Wireless Sensing Technologies	1 Bluetooth: Concepts of Pico net, Scatter net, Link types. Application of Blue tooth with Sensors. IEEE P1451standard	3	02	05
	2 ZigBee: components, architecture PLE, Self-Organizing networks and Applications with Sensors		01	
	3 Near Field Communication (NFC) and RFID: technical requirements, components and characteristics and their applications with Sensors		02	
5. Data Acquisition and Signal Conditioning	1 Signal Conditioning: Block Diagram of Signal Conditioning System, ADC, R2R DAC, Instrumentation Amplifier, Supervisory System (SCADA)	4	02	08
	2 Fundamentals of Data Acquisition: Analog and Digital data acquisition system with different configurations, Data loggers, Noise and interference	5	03	
	3 Utilization of Signal conditioning circuits for Temperature, Pressure, Optical, Strain gauges, Displacement and Piezoelectric Transducers		03	
6. Sensor Applications	1 On-board Automobile sensing system, Home appliances sensors, Aerospace Sensors, Sensors for Environmental Monitoring, Biomedical Sensing Applications.	6	04	08
	2 Radio sensors for industrial applications, Remote Sensing, Ground Penetrating Radars, Underwater sensing, Agricultural Sensor applications.		04	
. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01

Module No.	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
			Total:	**42**

Books:	
Text Books	1. An Introduction to Micro electromechanical Systems Engineering, 1st Edition, Nadim Maluf, Kirt Williams, Artech House 2004 2. Micro Electro Mechanical System Design, 2nd Edition, James J. Allen, Taylor and Francis, 2005 3. A Course in Electrical and Electronic Measurements and Instrumentation, 19th Edition, A K Swahney, Dhanpatrai & Co., 2011 4. Instrumentation Devices and System, 2nd Edition, Rangan, Mani and Sharma, Tata McGraw-Hill Publications, 1997
Reference Books	1. Sensors, Actuators and their Interfaces: A Multidisciplinary Introduction, 3rd Edition, Nathan Ida Wiley, 2010 2. Handbook of Modern Sensors Physics, Designs, and Applications, 4th Edition, Jacob Fraden Springer, 2010
Useful Links:	
1. https://nptel.ac.in/courses/108/108/108108147/ 2. https://www.youtube.com/watch?v=vjhp0zTXEsc 3. http://nptel.ac.in/courses/112103174/3	

Continuous Assessment (CA):
The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks):
Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment.

Internal Assessment(IA):
Marks will be awarded based on the rubrics designed.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Department Level Elective Course - I	Credits (TH+P+TUT)
EXDLC5053	**Microelectronics Devices and Circuits**	**3+0+0**
Prerequisite:	1. Electronic Devices and Circuits 2. Electrical Networks	
Course Objectives:	1. To give exposure to MOSFET devices and issues related to it. 2. To introduce Analog integrated circuits based on MOSFET 3. To give exposure to Analog IC design issues 4. To introduce Novel devices and circuits	
Course Outcomes:	1. Explain Model of FET devices 2. Analyze advanced amplifier circuit 3. Evaluate circuit parameter of given circuit 4. Design amplifier circuit for given overheads. 5. Explain working Novel devices and circuit 6. Evaluate capacitance and other physical parameter from Layout of simple integrated circuits	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
. MOSFET and scaling	MOS capacitor CV characteristic and concept of accumulation, depletion and inversion; MOSFET characteristics and SPICE models, Long channel and short channel MOSFET , Short channel effects	1	03	06
	Transistors along with mask layout diagram, Multi finger transistor, Scaling of MOSFET, CMOS technology	1,6	03	
. Current Mirror and DC analysis	Current Mirror, cascade current source, Wilson current source, bias independent current source using MOSFET	2,3	02	06
	DC analysis and small signal analysis of MOS active load, Differential pair, DC analysis and small signal analysis of MOS advanced active load amplifier, Differential pair	3,4	04	
. Amplifier with Active loads	CS amplifier with current source load, CS amplifier with diode connected load, CS amplifier with current source load, Common gate circuit	2,4	03	07

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	2 Differential pair, Cascode amplifier, Double Cascoding, Folded Cascod	2,3	04	
. **Frequency Response**	. Poles and Zeros of CS amplifier, Miller's Theorem, Direct analysis technique, impedance vs frequency	2	04	07
	2 Frequency response of single stage (CS, CG) amplifier. cascode stage, differential stage	2, 4,6	03	
. **Feedback in Circuits**	. Loop gain, feedback characteristic, Positive feedback, oscillator Barkhausen's criteria and oscillator example	5	02	07
	2 Negative feedback topology: voltage-voltage, voltage-current, current-current, current-voltage fed	3	03	
	3 Problem of instability in circuit, Stability analysis of Cascode circuit, Frequency Compensation, miller compensation	3,4	02	
. **Introduction of Novel Devices and circuit Design**	. Introduction to FinFet, GAA FETS, double gate, SOI multigate Mosfet	1, 5,6	02	06
	2 Analog Design: Device figure of merit, technology issue in circuit design, Flicker noise, matching behaviour and techniques, Layout rules for transistor matching		04	
. **Course Conclusion**	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**42**

Books:	
Text Books	1. D. A. Neamen, "Electronic Circuit Analysis and Design," Tata McGraw Hill, 2nd Edition 2. A. S. Sedra, K. C. Smith, and A. N. Chandorkar, "Microelectronic Circuits Theory and Applications," International Version, OXFORD International Students, 6th Edition 3. Behzad Razavi, Microelectronics, 2nd Edition
Reference Books	1. Behzad Razavi, Analog Circuit Design, 2nd Edition 2. J.P. Coligne Finfet and other Multi-Gate Transistors
Useful Links:	
1. https://www.semiconductors.org/semiconductors-101/what-is-a-semiconductor/ 2. https://onlinecourses.nptel.ac.in/noc21_ee51/ 3. http://cmosedu.com/	

Continuous Assessment (CA):
The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks):
Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment.

Internal Assessment(IA):
Marks will be awarded based on the rubrics designed.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	**Department Level Elective Course – I**	**Credits (TH+P+TUT)**
EXDLC5054	**Data Structures and Algorithms**	**3+0+0**
Prerequisite:	Computer Programming	
Course Objectives:	1. To introduce the fundamental knowledge & need of Data Structures. 2. To abstract the concept of Algorithm and these concepts are useful in problem solving. 3. To implement fundamental knowledge and applications of Stack, Queue, Linked List, Trees, Graphs etc. 4. To understand the working of different Sorting, Searching & Hashing techniques. 5. To understanding about writing algorithms and step by step approach in solving problems with the help of fundamental data structures. 6. To understand implementation of various strategies like divide and conquer, Dynamic programming.	
Course Outcomes:	1. Compare functions using asymptotic analysis and describe the relative merits of worst-, average-, and best-case analysis. 2. Apply various operations on Stack and Queue. 3. Ability to demonstrate the operation of Linked list 4. Ability to demonstrate and apply Trees & Graph data structures. 5. Familiarize with various Sorting- Searching and hashing Algorithms. 6. Ability to analyse different dynamic programming problems.	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
i. Prerequisites and Course Outlines	Control Structures, Arrays, Recursion, Pointers, Memory Allocation Techniques.	-	02	02
. Introduction to Data Structures and Algorithms	Introduction to Data Structures, Concept of ADT, Types of Data Structures: Linear and Nonlinear, Operations on Data Structures.	CO1	02	05
	Algorithm: Performance characteristics of algorithm, Importance of Algorithm Analysis, Complexity of an Algorithm, Introduction to Asymptotic Analysis and Notations.		03	
2. Stack & Queue	Introduction to Stack, ADT of Stack, Operations on Stack, Array Implementation of Stack	CO2	2	08
	Applications of Stack- Infix to Postfix Expression Conversion, Infix Expression to Prefix Expression Conversion, Postfix Expression Evaluation		2	
	Introduction to Queue, ADT of Queue, Operations on Queue, Array Implementation of Queue, Types of Queue-Circular Queue, Priority Queue, Introduction to Double Ended Queue		3	
	2.4 Applications of various types of Queue		1	
3. Linked List	Introduction to Linked list, Linked List v/s Array, Representation of Linked List, Types of Linked List - Singly Linked List, Doubly Linked List.	CO3	2	07
	Operations on Singly Linked List and Doubly Linked List		2	
	Singly Linked List Application-Polynomial Representation and Addition, Doubly Linked List Application		3	
. Trees & Graph	**Trees:** Introduction, Tree Terminologies, Binary Tree, Binary Tree Representation, Types of Binary Tree, Binary Tree Traversals, Binary Search Tree, Operations on Binary Search Tree,	CO4	2	09
	Applications of Binary Tree- Expression Tree, Huffman Encoding.		2	

Module No. & Name	Sub Topics	CO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Graph: Introduction, Graph Terminology, Memory Representation of Graph, Operations Performed on Graph.		2	
	Graph Traversal, Breadth First Search, Depth First Search, Applications of the Graph, Shortest Path, Minimum Spanning Tree.		3	
. Searching –Sorting and Hashing Algorithms	**Searching:** Sequential Search, Index Sequential Search, Binary Search**.**	CO5	2	6
	5.2 **Sorting:** Bubble Sort, Quick Sort, Merge Sort.		2	
	3 **Hashing:** Hashing-Concept, Hash Functions, Common hashing functions, Collision resolution Techniques.		2	
6. Dynamic Programming	All pair shortest path (Floyd-Warshall algorithm), Single source shortest path, (Dijkstra's Algorithm), 0/1 knapsack, Travelling salesman problem.	CO6	4	4
ii. Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
Total:				**42**

Books:	
Text Books	1. Data Structures A Psedocode Approach with C, Richard F. Gilberg & Behrouz A. Forouzan, Second edition, CENGAGE Learning 2. Data Structures using C, Reema Thareja, Oxford University press 3. Introduction to Data Structure and its Applications Jean-Paul Tremblay, P. G. Sorenson 4. Ellis Horowitz, Sartaj Sahni, S. Rajsekaran. "Fundamentals of computer algorithms" University Press 5. T.H.Coreman , C.E. Leiserson, R.L. Rivest, and C. Stein, "Introduction to algorithms", 2nd edition , PHI publication 2005. **6.** Alfred v. Aho, John E. Hopcroft , Jeffrey D. Ullman , "Data structures and Algorithm" Pearson education, Fourth impression 2009
Reference Books	1. Data Structures Using C & C++, Rajesh K. Shukla, Wiley- India 2. Data Structures Using C, ISRD Group, Second Edition, Tata McGraw-

	Hill 3. Data Structure Using C, Balagurusamy 4. C & Data Structures, Prof. P.S. Deshpande, Prof. O.G. Kakde, Dreamtech press 5. Data Structures, Adapted by: GAV PAI, Schaum's Outlines 6. Michael Gooddrich & Roberto Tammassia, "Algorithm design foundation analysis and internet examples", Second edition , Wiley student edition

Useful Links:

1. https://learndsa.kjsieit.in/
2. https://nptel.ac.in/courses/106/102/106102064/
3. https://www.coursera.org/specializations/data-structures-algorithms
4. https://www.edx.org/course/data-structures-fundamentals
5. https://swayam.gov.in/nd1_noc19_cs67/preview

Continuous Assessment (CA):

The distribution of Continuous Assessment marks will be as follows –

1.	Class Test 1 (T-1)	30 marks
2.	Class Test 2 (T-2)	30 marks
3.	Internal Assessment	10 marks

Class Tests (30 Marks):

Two class tests of 30 marks each should be conducted in a semester. The first class test is to be conducted when approx. 40% syllabus is completed and second class test when additional 40% syllabus (but excluding contents covered in Test I) is completed. Duration of each test shall be one hour and 15 Minutes. Average of the two class tests (T-1 and T-2) will be considered for Continuous Assessment.

Internal Assessment(IA):

Marks will be awarded based on the rubrics designed.

End Semester Theory Examination will be of 60 Marks with Two Hours and 30 Minutes duration.

Course Code	Course Name	Credits (P+TUT)
EXL501	**Digital Communication Laboratory**	**1+0**

Lab Prerequisite:	1. Analog communication 2. Electronic devices and circuits
Lab Objectives:	1. To learn source coding and error control coding techniques 2. To compare different line coding methods 3. To distinguish various digital modulations 4. To use different simulation tools for digital communication applications

Lab Outcomes:	1. Compare various source coding schemes 2. Design and implement different error detection codes 3. Illustrate the impulse response of a matched filter for optimum detection 4. Demonstrate various digital modulation techniques 5. Write accurate documentation for experiments performed 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory

Lab No.	**Experiment Title**	**LO Mapped**	**Hrs/ Lab**
0	Lab Prerequisites	-	02
1	Huffman code generation	1,5,6	02
2	Shannon-Fano code generation	1,5,6	02
3	Vertical redundancy Check (VRC) code generation and error detection	2,5,6	02
4	Horizontal Redundancy Check (HRC) code generation and error detection	2,5,6	02
5	Cyclic redundancy Check (CRC) code generation and error detection	2,5,6	02
6	Checksum code generation and error detection	2,5,6	02
7	Compare the performances of HRC and Checksum	2,5,6	02
8	Linear block code generation and error detection	2,5,6	02
9	Error detection and correction using Hamming code (virtual lab http://vlabs.iitb.ac.in/vlabsev/labs/mit_bootcamp/comp_networks_sm/labs/exp1/index.php)	2,5,6	02
10	Cyclic code generation and error detection	2,5,6	02
11	Convolutional code generation	2,5,6	02
12	Line Codes generation and performance comparison	1,5,6	02
13	Spectrum of line codes (NRZ unipolar and polar)	1,5,6	02
14	Impulse responses of ideal (Nyquist filter) and practical (Raised cosine filter) solution for zero ISI	3,5,6	02
15	Matched filter impulse response for a given input	3,5,6	02
16	Generation (and detection) of Binary ASK	4,5,6	02
17	Generation (and detection) of Binary PSK	4,5,6	02
18	Generation (and detection) of Binary FSK	4,5,6	02
19	Generation (and detection) of QPSK	4,5,6	02
20	Generation (and detection) of M-ary PSK	4,5,6	02
21	Generation (and detection) of M-ary FSK	4,5,6	02
22	Generation (and detection) of 16-ary QASK	4,5,6	02
23	Generation (and detection) of MSK	4,5,6	02
		Total	**48***
***Minimum 28 Hrs. Lab / Mini Project to be conducted**			
Suggested list of experiments is given as 23 experiments. One can add / subtract then this according to the syllabus and time. Term work should consist of minimum 8 experiments.			

Virtual Lab Links: http://vlabs.iitb.ac.in/vlabs-dev/labs/mit_bootcamp/comp_networks_sm/labs/exp1/index.php)
Term work: Term work should consist of a minimum of 8 experiments. Journal must include assignments on content of theory and practical of the course. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work. Total 25 Marks (Experiments: 15-marks, Assignments/ Case study/ Project/ demo/ presentation: 10-marks)
Oral/Practical/P&O : **Practical** examination will be based on the experiment list and content of the entire theory syllabus and carries 25-Marks

Course Code	Course Name	Credits (P+TUT)
EXL502	**Digital VLSI Digital Laboratory**	**1 + 0**

Lab Prerequisite:	Digital Logic Design
Lab Objectives:	1. To simulate the various phenomenon related to CMOS circuits 2. To analyse simple CMOS circuits using SPICE tools 3. To simulate the logic circuits using various design style 4. To draw mask layout of various circuits
Lab Outcomes:	1. Implement SPICE model for given combinational and sequential CMOS circuits. 2. Perform various analysis like operating point, dc, transient etc. of given CMOS circuits. 3. Design, simulate, and verify CMOS circuit for given specification and Evaluate performance of the same. 4. Draw layout of given CMOS circuit and also able extract various parasitic using open source layout tool like Magic. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Constant Voltage and Constant field MOSFET scaling	2,5,6	02
2	Layout of MOSFET and extraction of parasitic capacitances	4,5,6	02

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
3	Voltage transfer characteristics of CMOS inverter and calculation of Noise Margin and static power	2,5,6	02
4	Transient Analysis of CMOS inverter and calculation of t_{pHL}, t_{pLH}, t_r, t_f and average power	3,5,6	02
5	Design of CMOS inverter for given specifications	3,5,6	02
6	Layout of CMOS inverter and comparison of pre layout and post layout performance	4,5,6	02
7	Voltage transfer characteristics of 2 input NAND/NOR gate and calculation of noise margins and validation using equivalent inverter approach	2,5,6	02
8	Transient Analysis of 2 input NAND/NOR CMOS gate and calculation of t_{pHL}, t_{pLH}, t_r, t_f, average power and validation using equivalent inverter approach	3,5,6	02
9	Layout of 2 input CMOS NAND/NOR gate and comparison of pre layout and post layout performance	4,5,6	02
10	Static and transient analysis of Complex CMOS gate	3,5,6	02
11	Layout of complex CMOS gate using Euler path	4,5,6	02
12	Implementation of various combinational and sequential circuits using different design styles	1,5,6	02
13	Design and implementation of NAND based and NOR based ROM array	3,5,6	02
14	Performance analysis of 6T-SRAM Cell	3,5,6	02
15	Design of 6T SRAM cell robust read and write operation	3,5,6	02
16	Performance analysis of 1T and 3T DRAM Cell	3,5,6	02
17	RTL design of Soda dispenser machine	1,5,6	02
18	RTL design of FIR Filter	1,5,6	02
		Total	**38***
***Minimum 28 Hrs. Lab / Mini Project to be conducted**			
Virtual Lab Links: https://vlsi-iitg.vlabs.ac.in/			

Term work:

1. Term work should consist of a minimum of 8 experiments.
2. Journal must include assignments on content of theory and practical of the course.
3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/ Case study /Project/ demo/ presentation: 10-marks)

Oral/Practical/P&O :
Practical examination will be based on the experiment list and content of the entire theory syllabus and carries 25-Marks

Course Code	Course Name	Credits (P+TUT)
EXL503	**Discrete Time Signal Processing Laboratory**	**1+0**

Lab Prerequisite:	Signals and Systems
Lab Objectives:	1. To carry out basic discrete time signal processing operations 2. To implement and design FIR filters and IIR filters 3. To implement applications related to the field of biomedical signal processing and audio signal processing
Lab Outcomes:	1. Demonstrate their ability to perform frequency analysis of different discrete time sequences. 2. Perform basic signal processing operations such as circular convolution of discrete time sequences. 3. Design and implement IIR & FIR Filters for given specifications. 4. Analyse and Implement applications related to the field of biomedical signal processing and audio signal processing 5. Write accurate Documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Impulse response of Discrete Time System	1,5,6	02
2	4-point DFT of Discrete Time Sequence	1,5 ,6	02
3	Circular Convolution of Discrete Time Sequence	1,2,5,6	02
4	8- point DFT of Discrete Time Sequence	1,5,6	02
5	Butterworth IIR filter using Impulse Invariance Transformation	3,5,6	02
6	Butterworth IIR filter using Bilinear Transformation Technique	3,5,6	02
7	Chebyshev filter using Bilinear Transformation Technique	3,5,6	02
8	Impulse response of FIR band pass filter	3,5,6	02

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
9	Impulse FIR filter using Rectangular Window	3,5,6	02
10	Case study on different applications of Digital Signal Processing	4,5,6	08
		Total	**28**

Virtual Lab Links:
vlabs.iitkgp.ernet.in/dsp/#

Term work:

1. Term work should consist of a minimum of 8 experiments.
2. Journal must include assignments on content of theory and practical of the course.
3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/Project/demo/presentation: 10-marks)

Course Code	Department Level Elective Course – I Laboratory	Credits (P+TUT)
EXDLL5051	**Data Compression and Encryption Laboratory**	**1+0**

Lab Prerequisite:	Any suitable programming skills
Lab Objectives:	To apply statistical and dictionary methods for text compression To understand on how to apply the concept of quantization and audio/image compression To understand the concepts of Encryption and techniques of Encryption To understand on how to apply the cryptographic algorithm
Lab Outcomes:	1. Implement Text compression Techniques 2. Implement Image compression techniques 3. Implement data Encryption technique 4. Implement public key cryptography algorithms 5. Write accurate documentation for experiments performed 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02

1	Write a program to encode and decode message and find code efficiency using Arithmetic Coding	1,5,6	02
2	Write a program to encode and decode the text using Dictionary methods	1,5,6	02
3	Write a program to Discrete Cosine Transform for image compression	2,5,6	02
4	To study DPCM Audio Compression Method	2,5,6	02
5	To study the effect of Uniform and Non uniform Quantization on speech signal	2,5,6	02
6	Write a program to apply Affine Cipher Encoding and decoding for data encryption	3,5,6	02
7	Write a program to apply Caesar Cipher Encoding and decoding for data encryption	3,5,6	02
8	Write a program to implement Diffie-Hellman Public Key Cryptography	4,5,6	02
9	To study RSA Public Key Encryption and Decryption Algorithm	4,5,6	02
10	To study the Message Authentication algorithm	4,5,6	02
11	Case Study / Mini Project	1,2,3,4,5,6	06
		Total	**28**

Virtual Lab Links:
1/cse29-iiith.vlabs.ac.in/

Term work:

1. Term work should consist of a minimum of 8 experiments.
2. Journal must include assignments on content of theory and practical of the course.
3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/Project/demo/presentation: 10-marks)

Course Code	**Department Level Elective Course – I Laboratory**	**Credits (P+TUT)**
EXDLL5052	**Sensor Technology Laboratory**	**1+0**

Lab Prerequisite:	1. Knowledge of implementing Electronic Circuits 2. Interfacing devices for processing such as Arduino, Raspberry Pi, Microprocessors and Microcontrollers. 3. Signal Conditioning Circuits

Lab Objectives:	1. To implement basic applications using different types of Sensors. 2. To apply the knowledge of MEMS and Smart sensors by implementing applications 3. To implement signal conditioning circuits to shape the input signals. 4. To interface sensors with various communication Technologies
Lab Outcomes:	1. Develop basic sensor application circuit using sensors like temperature, smoke, humidity, moisture sensors. 2. Apply the smart sensors and connect them to different platforms like wired and wireless. 3. Design suitable signal conditioning to different types of sensor outputs for further processing. 4. Implement applications based on A to D convertors and D to A convertors and connect them to sensor circuits through different case studies. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Study of different types of sensors by observing them in the lab and study the important parameters like accuracy, Precision, Resolution, Range, tolerance limits etc.	1,5,6	02
2	Implement a circuit to detect smoke.	1,5,6	02
3	Design bimorph cantilever which acts as a pressure sensor.	2,5,6	02
4	Model and simulate Electro-mechanical actuator. Do dc and transient analysis	2,5,6	02
5	Simulate the harvested electrical power from mechanical vibrations using piezoelectric cantilever beam.	2,5,6	02
6	Model and simulate accelerometer	2,5,6	02
7	Implement A to D conversion	3,5,6	02
8	Implement R2R D to A convertors	3,5,6	02
9	Interfacing the Zigbee with humidity sensors.	4,5,6	02
10	Interfacing RFID with proximity sensors	4,5,6	02
11	Study of NFC and suitable sensors for interfacing.	4,5,6	02
12	Case Study / Mini Project	1 to 6	04
		Total	**28**

Virtual Lab Links:
https://ssp-iitb.vlabs.ac.in/

Term work:

1. Term work should consist of a minimum of 8 experiments.
2. Journal must include assignments on content of theory and practical of the course.
3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/ Case study/ Project/ demo/ presentation: 10-marks)

Course Code	Department Level Elective Course – I Laboratory	Credits (P+TUT)
EXDLL5053	**Microelectronics Devices and Circuits Laboratory**	**1 + 0**
Lab Prerequisite:	Electronic Devices & Circuits	
Lab Objectives:	. To provide insight into Analog circuit design using CAD tools . To gain proficiency in integrated circuit analysis using LTspice . To provide exposure to Layout IC design . To provide insight into Analog design flow process	
Lab Outcomes:	1. Design amplifier circuits in LTspice simulation environment. 2. Design layout of amplifier inverter in Electric 3. Analyse from the data available from simulation in LTspice 4. Asses different circuit and device models 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the Laboratory	

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
0	Lab Prerequisites	-	02
1	Installations and demonstration of CAD Design software: types, working roles in IC design	5,6	02
2	Plot long and short channel MOSFET characteristics	3,4,5,6	02
3	DC analysis of advance active load amplifier	3,4,5,6	02
4	DC analysis of Cascode amplifier	3,4,5,6	02
5	Transient analysis of Cascode amplifier	3,4,5,6	02
6	AC Analysis of Cascode amplifier	3,4,5,6	02
7	AC analysis of Differential amplifier	3,4,5,6	02
8	CMOS inverter simulation	3,4,5,6	02
9	CMOS inverter Layout simulation, DRC, LVS steps.	2,5,6	02
10	Layout of CS amplifier	2,5,6	02
11	Implement available Compact model equation in octave	3,5,6	02
12	Implementation of CAD Design software using simple	5,6	02

	techniques/available open source software for mobile devices		
13	Study of Verilog-A software and design flow	5,6	02
		Total	**28**

Virtual Lab Links:

1. http://vlabs.iitkgp.ernet.in/be/
2. http://cmosedu.com/
3. https://www.youtube.com/watch?v=rXTEmojksd4

Term work:

1. Term work should consist of a minimum of 8 experiments.
2. Journal must include assignments on content of theory and practical of the course.
3. The final certification and acceptance of term work ensures satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/Project/demo/presentation: 10-marks)

Course Code	**Department Level Elective Course– I Laboratory**	**Credits (P+TUT)**
EXDLL5054	**Data Structures and Algorithm Laboratory**	**1+0**

Lab Prerequisite:	1. Computer Programming 2. Computer Programming Laboratory
Lab Objectives:	1. To implement basic data structures such as linked lists, stacks and queues 2. To solve problem involving graphs and trees 3. To choose appropriate data structure and apply it to various problems
Lab Outcomes:	1. Choose appropriate data structure as applied to specify problem definition and to select appropriate problem solving strategies. 2. Use linear and non-linear data structures like stacks, queues, linked list etc. 3. Calculate time complexity and space complexity of an algorithm. 4. Analyse different divide and conquer problems, dynamic programming problems. 5. Write accurate documentation for experiments performed. 6. Apply ethical principles like timeliness and adhere to the rules of the laboratory.

Lab No.	**Experiment Title**	**LO Mapped**	**Hrs/ Lab**
0	Lab Prerequisites	-	02
1	Implementations of stack menu driven program	1,5,6	02

Lab No.	Experiment Title	LO Mapped	Hrs/ Lab
2	* Implementations of Infix to Postfix Transformation and its evaluation program	2,5,6	02
3	Implementations of queue menu driven program	1,5,6	02
4	* Implementations of double ended queue menu driven program	1,2,5,6	02
5	* Implementation of different operations on linked list – copy, concatenate, split, reverse, count no. of nodes etc.	1,2,5,6	02
6	Implementation of polynomials operations (addition, subtraction) using Linked List	2,5,6	02
7	*Implementations of Binary Tree menu driven program	2,5,6	02
8	*Implementation of construction of expression tree using postfix expression.	3,5,6	02
9	* Implementations of Graph menu driven program (DFS & BSF)	3,5,6	02
10	Write a program for a. selection sort b. insertion sort	3,5,6	02
11	* Write a program using Divide and Conquer for a. Merge sort analysis b. Quick sort analysis	4,5,6	02
12	Write a program using Divide and Conquer for a. binary search b. finding minimum and maximum	4,5,6	02
13	*Write a program for Optimal binary search tree using dynamic programming	4,5,6	02
14	*Write a program for Travelling salesman problem using dynamic programming	4,5,6	02
		Total	**30**
* Compulsory / **Minimum 28 Hrs. Lab / Mini Project to be conducted**			
Useful Links:			
1. https://www.programiz.com/dsa 2. https://www.codechef.com/certification/data-structures-and-algorithms/prepare			

rm work:

1. Term work should consist of a minimum of 8 experiments
2. Journal must include assignments on content of theory and practical of the course
3. The final certification and acceptance of term work ensures that satisfactory performance of laboratory work and minimum passing marks in term work.
4. Total 25 Marks (Experiments: 15-marks, Assignments/Case study/demo/presentation: 10-marks

Course Code	Course Name	Credits (TH+P+TUT)

EXL506	Business Communication & Ethics Laboratory	0+2+0
Hardware Requirements:	PC With following Configuration 1. Intel Dual core Processor or higher 2. Minimum 4 GB RAM 3. Minimum 40 GB Hard disk	
Software Requirements:	1. Microsoft Windows 10 Desktop OS 2. Language Laboratory Software: ODLL (Orell Digital Language Laboratory)	
Lab Prerequisite:	Fundamental knowledge of Professional Communication Skills as acquired in semester II	
Course Rationale:	This curriculum is designed to build up a professional and ethical approach, effective oral and written communication with enhanced soft skills. Through practical sessions, it augments student's interactive competence and confidence to respond appropriately and creatively to the implied challenges of the global Industrial and Corporate requirements. It further inculcates the social responsibility of engineers as technical citizens.	
Lab Objectives:	1. To discern and develop an effective style of writing important technical/business documents 2. To investigate possible resources and plan a successful job campaign 3. To comprehend the dynamics of professional communication in the form of group discussions, meetings, etc. required for career enhancement 4. To develop creative and impactful presentation skills 5. To ehavio personal traits, interests, values, aptitudes and skills 6. To understand the importance of integrity and develop a personal code of ethics	
Lab Outcomes:	1. Plan and prepare effective business/ technical documents, which will in turn provide a solid foundation for their future managerial roles. 2. Strategize their personal and professional skills to build a professional image and meet the demands of the industry. 3. Emerge successful in group discussions, meetings and result-oriented agreeable solutions in-group communication situations. 4. Deliver persuasive and professional presentations. 5. Develop creative thinking and interpersonal skills required for effective professional communication 6. Apply codes of ethical conduct, personal integrity and norms of organizational behaviour	

Module No. & Name	Sub Topics	TO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
Prerequisites and Course Outlines	Prerequisite Concepts and Course Introduction	-	02	02
. Advanced Technical Writing:	1. Classification of Reports: Classification on the basis of:	1, 6	01	06

Module No. & Name	Sub Topics	TO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
Project/ Problem Based Learning	Subject Matter (Technology, Accounting, Finance, Marketing, etc.) Time Interval (Periodic, One-time, Special) Function (Informational, Analytical, etc.) Physical Factors (Memorandum, Letter, Short & Long)			
	2. Parts of a Long Formal Report: Prefatory Parts (Front Matter) Report Proper (Main Body) Appended Parts (Back Matter)		01	
	3. Language and Style of Reports Tense, Person & Voice of Reports Numbering Style of Chapters, Sections, Figures, Tables and Equations Proofreading through Plagiarism Checkers		01	
	4. Definition, Purpose & Types of Proposals Solicited (in conformance with RFP) & Unsolicited Proposals Types (Short and Long proposals)		01	
	5. Parts of a Proposal Elements Scope and Limitations Conclusion		01	
	6. Technical Paper Writing Parts of a Technical Paper (Abstract, Introduction, Research Methods, Findings and Analysis, Discussion, Limitations, Future Scope and References) Language and Formatting Referencing in IEEE Format		01	
Employment Skills	2.1. Cover Letter & Resume Parts and Content of a Cover Letter Difference between Bio-data, Resume & CV Essential Parts of a Resume Types of Resume (Chronological,	2, 4	01	06

Module No. & Name	Sub Topics	TO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Functional & Combination)			
	2.2 Verbal Aptitude Test Modelled on CAT, GRE, GMAT exams		01	
	2.3 Group Discussions Purpose of a GD Parameters of Evaluating a GD		01	
	Types of GDs (Normal, Case-based & Role Plays)		01	
	GD Etiquettes		01	
	2.4 Personal Interviews Planning and Preparation Types of Questions Types of Interviews (Structured, Stress, Behavioural, Problem Solving & Case-based) Modes of Interviews: Face-to-face (One-to one and Panel) Telephonic, Virtual		01	
. Business Meetings	3.1 Conducting Business Meetings Types of Meetings Meeting etiquettes	3, 6	01	02
	3.2 Documentation Notice Agenda Minutes		01	
4. Technical/ Business Presentations	4.1 Effective Presentation Strategies Defining Purpose Analyzing Audience, Location and Event Gathering, Selecting & Arranging Material	2, 4	01	02
	4.2 Structuring a Presentation Making Effective Slides Types of Presentations Aids Closing a Presentation		01	
. Interpersonal Skills	Emotional Intelligence	5, 6	01	08
	Motivation		01	
	Assertiveness		01	
	Time Management		02	
	Stress Management		02	
	5.2 Start-up Skills	2, 5	01	

Module No. & Name	Sub Topics	TO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
	Financial Literacy Risk Assessment Data Analysis (e.g. Consumer Behaviour, Market Trends, etc.)			
6. Corporate Ethics	6.1 Intellectual Property Rights Copyrights Trademarks Patents	6	01	02
	6.2 Case Studies Cases related to Business/ Corporate Ethics	1 to 6	01	
Course Conclusion	Recap of Modules, Outcomes, Applications and Summarization.	-	01	01
			Total:	**28**

Activity No.	Activity/ Assignment Title (In the form of Short Notes, Questionnaire/ MCQ Test, Role Play, Case Study, Quiz, etc.)	Hrs/ Lab
	Test of English as Foreign Language (TOEFL)	02
	Group discussion (Practice session)-I	02
	Group discussion (Practice session)-II	02
	Final Group discussion-I	02
	Final Group discussion-II	02
	English Aptitude Test	02
	Resume Writing	02
	Mock interview	02
	Role play techniques for interpersonal skills	02
	Project Report Presentation-I	02
	Project Report Presentation -II	02
	Technical proposal	02
13.	Corporate Ethics/role play/case studies	02
	Business Meetings: case studies/role play	02
	Total:	**28**

Books:	
Text Books	1. Sanjay Kumar & PushpLata (2018). Communication Skills a workbook, New Delhi: Oxford University Press. 2. Bovée, C. L., & Thill, J. V. (2021). *Business communication today*. Upper Saddle River, NJ: Pearson.

Reference Books	1. Arms, V. M. (2005). Humanities for the engineering curriculum: With selected chapters from Olsen/Huckin: Technical writing and professional communication, second edition. Boston, MA: McGraw-Hill. 2. Butterfield, J. (2017). Verbal communication: Soft skills for a digital workplace. Boston, MA: Cengage Learning. 3. Masters, L. A., Wallace, H. R., & Harwood, L. (2011). Personal development for life and work. Mason: South-Western Cengage Learning. 4. Robbins, S. P., Judge, T. A., & Campbell, T. T. (2017). Organizational behaviour. Harlow, England: Pearson. 5. Meenakshi Raman, Sangeeta Sharma (2004) Technical Communication, Principles and Practice. Oxford University Press 6. Archana Ram (2018) Place Mentor, Tests of Aptitude for Placement Readiness. Oxford University Press

Useful Video links:

1. TOEFL listening Skill
ttps://www.youtube.com/watch?v=jSUh0Civuv4
2. MBA Interview
https://www.youtube.com/watch?v=cwW9QBNuwCw
3. How to write a successful CV
https://www.youtube.com/watch?v=U0JAfqEak2c
4. Interview techniques (How to answer tell me about yourself)
https://www.youtube.com/watch?v=m5kR7TPAkSw
5. The 4 types of team members you can hire
https://www.youtube.com/watch?v=5bYYFfpbSqc
6. Every Meeting Ever
https://www.youtube.com/watch?v=K7agjXFFQJU

Assessment:

Term Work (25 Marks)

Term work of 25 Marks shall consist of a minimum 8 Assignments.
The distribution of marks for term work shall be as follows:
Assignment: 15 Marks
Book Report (hard copy): 10 Marks
Note: The final certification and acceptance of term work ensures the satisfactory performance of laboratory work and minimum passing in the term work.

Oral (25 Marks)
Oral Examination will be based on a GD & the Project/Book Report presentation.

1	Group Discussion: 10 Marks
2	Project Presentation: 15 Marks

Note:
1. The Main Body of the project/book report should contain a minimum **25 pages** (excluding Front and Back matter).
2. The group size for the final report presentation should not be less than 5 students or exceed 7 students.
3. There will be an end–semester presentation based on the book report.

Course Code	Project Based Learning	Credits (TH+P+TUT)
EXPR53	**Minor Project Lab – I**	**0 +1+ 0**
Prerequisite:	1. Microcontrollers 2. Linear Integrated Circuits 3. Mini Project 1B: Arduino & Raspberry Pi based Projects	
Minor Project Objectives:	1. To develop background knowledge of Embedded Systems. 2. To understand the design of embedded systems. 3. To choose proper microcontroller for Embedded systems 4. To understand use of wireless sensors/communications with Embedded systems 5. To understand communication techniques. 6. To write programs for embedded systems and real time operating systems / IoT	
Minor Project Outcomes:	1. Outline the embedded systems concept with design metrics 2. Outline microcontroller's concept. 3. Implement the Embedded systems with different sensors and peripherals as IoT. 4. Implement the Embedded systems with different communication protocols as IoT. 5. Analyse concepts of Real time operating systems. 6. Design embedded system applications using sensors, peripherals and RTOS	

Module No. & Name	Sub Topics	CO Mapped	Hrs / Sub Topic	Hrs / Topic
1. Introduction	1 Definition of Embedded System, Embedded Systems Vs General Computing Systems, Classification, Major Application Areas. Characteristics and quality attributes (Design Metric) of embedded system	1	02	04
	2 Identification of Project Title		02	
. Controller boards and Programm	1 ARM LPC 21XX (2148), STM32 boards and Texas MSP 430 lunchbox/ Tiva C board and PIC/PSoc*	2	01	04
	2 Comparison of C and embedded C, Data Types, Variable, Storage		01	

Module No. & Name	Sub Topics	CO Mapped	Hrs / Sub Topic	Hrs / Topic
ing – Embedded C	Classes, Bit operation, Arrays, Strings, Structure and unions, Classifier			
	3 Exercise: Identify the suitable board required for the particular application with respect to design metrics. (Hint: check clock frequency (speed), memory (program and data), no. of ports for peripherals, timers/counters and serial communication requirement for project)		01	
	4 Suggested Way to Identify: https://predictabledesigns.com/how-to-selectthe-microcontroller-for-your-new-product/		01	
. Interfacing Sensors and peripherals using Embedded C	1 Sensors and Signal Conditioning Circuits amplifiers /attenuators /filters /comparators/ADC and DAC) , Interfacing with GLCD/TFT display, Relays and Drivers for interfacing Motors (DC and stepper)	3	02	05
	2 Exercise: Understand the Interfacing requirement like drivers, signal condition circuits for sensors, etc. for the selected application		01	
	3 Study Material: For LCD interfacing with MSP430 Launch Pad https://microcontrollerslab.com/lcd-interfacing-msp430-launchpad/#:~:text=LCD%20interfacing%20with%20MSP430%20microcontroller,Now%20I%20will&text=It%20requires%205%20volts%20dc,and%20seco nd%20pin%20is%20vcc.		02	
. Communication with programming in Embedded C	1 Serial communication, CAN bus, I2C, MOD bus, SPI	4	01	05
	2 Interfacing with Wi-Fi, Bluetooth ,ZigBee, LoRa, RFID and putting data on IoT		01	
	3 Interfacing with GSM module , GPS module, SD card		01	
	4 Exercise: Understand Communication requirement for selected application and test it		01	
	5 STM32:https://controllerstech.com/serial-transmission-in-stm32/#:~:text=Serial%20Transmission%20in%20Stm32&text=UART%20is %20widely%20used%20for, amongst%20which%20communication%20is%20 done. LPC2148: https://www.electronicwings.com/arm7/lpc2148-uart0 MSP430: https://www.ti.com/lit/ml/slap117/slap117.pdf		01	
. Real Time Operating	1 Operating system basics, Types of OS , Tasks, process, Threads	5	02	04
	2 Multiprocessing and Multitasking, Task scheduling		01	

Module No. & Name	Sub Topics	CO Mapped	Hrs / Sub Topic	Hrs / Topic
Systems [RTOS]	3 RTLinux/ Free RTOS and Mbed OS, Implementation with RTOS		01	
. Cloud/ Web server	1 Implementation on web server	6	01	04
	2 Thingspeak, AWS cloud platform for IoT based programming and modelling		01	
	3 Exercise : Perform ESP8266 interface with microcontroller		01	
	4 Study Material: STM32: https://circuitdigest.com/microcontroller-projects/interfacingesp8266-with-stm32f103c8-stm32-to-create-a-webserver LPC2148: https://circuitdigest.com/microcontroller-projects/iot-based-ARM7- LPC2148-webserver-to-control-an-led MSP430: https://circuitdigest.com/microcontroller-projects/sending-emailusing-msp430-and-esp8266		01	
			Total	**26**

Books:	
Text Books	1. Shibu K.V," Introduction to Embedded Systems", Mc Graw Hill, 2nd edition. 2. Frank Vahid, and Tony Givargis, "Embedded System Design: A unified Hardware/Software Introduction", Wiley Publication. 3. Raj Kamal," Embedded Systems Architecture, Programming and design", Tata McGraw-Hill Publication. 4. 4. Dr. K.V.K.K. Prasad, "Embedded Real Time Systems: Concepts, Design & Programming", Dreamtech Publication.
Reference Books	1. Iyer, Gupta," Embedded real systems Programming", TMH 2. David Simon, "Embedded systems software primer', Pearson 3. Andrew Sloss, Dominic Symes and Chris Wright, "ARM_System_Developers_GuideDesigning_and_Optimizing_System_Software" Elsevier and Morgan Kaufmann Publishers.
Useful Links:	

1. Introduction to Embedded System Design (using MSP430) https://onlinecourses.nptel.ac.in/noc20_ee98/preview
2. Embedded System Design with ARM https://onlinecourses.nptel.ac.in/noc20_cs15/preview
3. Embedded systems https://nptel.ac.in/courses/108/102/108102045/
4. Master Microcontroller and Embedded Driver Development (MCU1) STM32 Udemy course link mastering microcontrollers with peripherals
5. Texas Instruments (TI)

Trainings: https://e2e.ti.com/support/archive/universityprogram/educators/w/wiki/2103/training-support

6. Texas Instruments (TI) Teaching material/ text books: https://e2e.ti.com/support/archive/universityprogram/educators/w/wiki/2035/textbooks

Continuous Assessment: Practical (25 Marks)

A. Guideline of Minor project are as follows :

1. To achieve proper selection of Minor Projects. Students should do a survey of different microcontroller board from given microcontroller series tools and identify which is most suitable for their selected topic. They should consult with their Guide/Mentors / Internal committee to finalize it.
2. Students shall submit implementation plan in the form of Smart Report/Gantt/PERT/CPM chart, which will cover weekly activity of minor project.
3. A logbook to be prepared by each group, wherein group can record weekly work progress. Guide/ supervisor will verify it and will put notes/comments.
4. Guide/supervisor guidance is very much important during minor project activities; however, focus shall be on self-learning.

Suggested steps for Minor project selection and implementation

Minor project should be completely microcontroller based

Follow these steps:

a. Take specification, using these specifications design project.

b. Select proper microcontroller board considering features and requirements of project.

c. Program it using Embedded C and perform verification of each module (sensors/communication protocol)

d. Test Functional Simulation and verify it using simulation tool.

e. Make hardware connection on GPP of peripherals with microcontroller board and execute the program.

f. Troubleshoot if not get expected result.

B. Project Topic selection and approval :

1. The group may be of maximum THREE (03) students.
2. Topic selection and approval by 2 Expert faculties from department at the start of semester.
3. Log Book to be prepared for each group to record the work progress in terms of milestones per week by students. Weekly comment, remarks to be put by guiding faculty. Both students and faculty will put signature in it per week. The log book can be managed online with proper authentication method using Google sheets/forms or open source project management software.

C. Project Report Format:

1. Report should not exceed 30 pages. Simply staple it to discourage use of plastic.
2. Report must contain block diagram, circuit diagram, screenshot of outputs and datasheets of microcontrollers and peripherals (Include only required information pages).
3. The recommended report writing format is in LaTex.(https://youtu.be/YLm3sXlKpHQ)

Term Work: (25 marks)

1. Term Work evaluation and marking scheme:

a. The review/ progress monitoring committee shall be constituted by Head of Departments of each institute.

b. The progress of minor project to be evaluated on continuous basis, minimum two reviews in each semester.

c. At end of semester the above 2 expert faculty who have approved the topic will internally evaluate the performance.

d. Students have to give presentation and demonstration on the Embedded Systems Minor Project at end of semester before submission to above experts.

e. In the evaluation each individual student should be assessed for his/her contribution, understanding and knowledge gained about the task completed. Based upon it the marks will be awarded to student.

f. Distribution of 25 Marks scheme is as follows:

i. Marks awarded by guide/supervisor based on log book and output: 10

ii. Marks awarded by review committee: 10

iii. Quality of Project report: 05

2. Guidelines for Assessment of Minor Project Practical/Oral Examination:

a. Report should be prepared as per the guidelines issued by the University of Mumbai.

b. Minor Project shall be assessed through a presentation and demonstration of working model by the student project group to a panel of Internal and External Examiners preferably from industry or research organisations having experience of more than five years approved by head of Institution.

Text Books:

1.Quantitative abilities by Arun Sharma

2. Quantitative Aptitude for Competitive Examinations by R S Agrawal

3. Verbal and Non-Verbal reasoning by R S Agrawal

4. Guide to Competitive Programming Learning and Improving Algorithms Through Contests Antti Laaksonen, Department of Computer Science, University of Helsinki, Finland

Reference Books:

1. Algorithms Illuminated by Tim Roughgarden

2. Algorithm Design, Jon Kleinberg and Éva Tardos 3. Introduction to Algorithms, Cormen, Leiserson, Rivest, Stein 4. Competitive Programming 4: The Lower Bound of Programming Contests in the 2020s by Steven Halim and Felix Halim 5. Guide to Competitive Programming: Learning and Improving Algorithms Through Contests Antti Laaksonen.
Useful Links: 1. https://doi.org/10.1007/978-3-319-72547-5 2. Algorithms by Jeff Erickson (freely available online) 3. https://onlinecourses.nptel.ac.in/noc21_cs99/preview 4. https://unacademy.com/a/i-p-c-beginner-track

Term Work (25 Marks): Marks will be awarded based on Assessment Rubrics: 1. Student's active participation in skill based learning. 2. Presenting/showcasing learned skills through Social /outreach/ extension activities/Events/ Competitions/Trainings/Internships etc. 3. Submission of Report/act/demonstrations/ specific participation/Idea creation/scope/creativity/Case study etc. 4. Achievement/Recognition.

Skill Based Learning Code	**Skill Based Learning - VII**	**Credits (TH+P+TUT)**
EXXS57	**Aptitude/Logic Building and Competitive Programming skills**	**0+1+0**
Skill Prerequisite	1. Knowledge of elementary mathematics (HSC level) 2. Knowledge of basic English grammar (SSC level) 3. Knowledge of Basic programming languages	

Skill Objectives	To have the basic awareness about how to prepare for recruitment process To introduce the students to computational skills required to appear for recruitment tests. To introduce the students to coding skills required to appear for recruitment tests/ project /coding competitions.

Skill Outcomes	1. Discuss the basic concepts of QUANTITATIVE ABILITY 2. Discuss the basic concepts of LOGICAL REASONING Skills 3. Acquire satisfactory competency in use of VERBAL REASONING 4. Solve campus placements aptitude papers covering Quantitative Ability, Logical Reasoning and Verbal Ability 5. Use most common algorithms for competitive programming 6. Analyse data structures for competitive up solving.

Module No & Name	Sub Topics	SO Mapped	Hrs/ Sub Topic	Total Hrs/ Module
. **Basics of Quantitative Abilities**	Problems on Number System Problems on HCF and LCM Problems on Average	1,4	02	06
	Problems on Ratio and Proportion, Problems on Percentage		02	
. **Arithmetic Quantitative Abilities**	Problems on Ages, Problems on Profit and Loss	1,4	02	06
	Problems on Simple and Compound Interest, Problems on Time and Distance		02	
. **Logical Reasoning**	Number Series, Alpha Numerical, Letter & Symbol Series	2,4	02	04
	Numerical and Alphabet Puzzles, Seating Arrangement			
. **Programming Techniques**	What is Competitive Programming? Programming Contests, Language Features	5	02	05
	Recursive Algorithms, Bit Manipulation		03	
Sorting and Searching	Sorting Algorithms, Solving Problems by sorting, Binary Search	6	05	05
. **Course Conclusion**	Course recap, Outcomes, Discussion	-	-	02
			Total:	**28**

Text Books:

1.Quantitative abilities by Arun Sharma

2. Quantitative Aptitude for Competitive Examinations by R S Agrawal

3. Verbal and Non-Verbal reasoning by R S Agrawal

4. Guide to Competitive Programming Learning and Improving Algorithms Through Contests Antti Laaksonen, Department of Computer Science, University of Helsinki, Finland

Reference Books:

1. Algorithms Illuminated by Tim Roughgarden
2. Algorithm Design, Jon Kleinberg and Éva Tardos
3. Introduction to Algorithms, Cormen, Leiserson, Rivest, Stein
4. Competitive Programming 4: The Lower Bound of Programming Contests in the 2020s by Steven Halim and Felix Halim
5. Guide to Competitive Programming: Learning and Improving Algorithms Through Contests

Antti Laaksonen.
Useful Links: 1. https://doi.org/10.1007/978-3-319-72547-5 2. Algorithms by Jeff Erickson (freely available online) 3. https://onlinecourses.nptel.ac.in/noc21_cs99/preview 4. https://unacademy.com/a/i-p-c-beginner-track
Term Work (25 Marks): Marks will be awarded based on Assessment Rubrics: 1. Student's active participation in skill based learning. 2. Presenting/showcasing learned skills through Social /outreach/ extension activities/Events/ Competitions/Trainings/Internships etc. 3. Submission of Report/act/demonstrations/ specific participation/ Idea creation/scope/creativity/Case study etc. **4.** Achievement/Recognition.

Technology Based Learning Code	**SAT Course**	**Credits**
EXXT58	**Technology Based Learning - VIII**	**0 – 1 – 0**
Prerequisite:	Basic Engineering and Technology courses	
TBL Objectives:	1. To acquire competency in emerging areas of technology. 2. To create a mind set for life-long learning required to persist technological shifts and be abreast with the market trends. 3. To facilitate learning at self-paced schedules. 4. To boost time management ability and self-discipline. 5. To provide opportunities of strengthening digital footprints by showcasing the additional proficiency acquired as well as improve connectivity and networking. 6. To enhance employment and entrepreneurial opportunities requiring specialization.	

TBL Outcomes:	1. Explain concepts of the emerging technology learned through the pursued course. 2. Describe social, ethical, and legal issues surrounding the learned technology. 3. Demonstrate professionalism and skills of digital age learning and working. 4. Demonstrate knowledge in entrance exams for higher technical education, placement interviews, and other avenues. 5. Analyse real-world case studies in society/industry for applicability of sustainable technological solutions. **6.** Apply the acquired knowledge in developing technology-based solutions to real-world problems or other projects at hand.

Guidelines for Technology Based Learning:

1. Learners should enrol for an online course based on their area of interest concerning emerging areas of technology in consultation with Faculty Supervisor nominated by the Head of Department.
2. The course duration should be of minimum 04 weeks.
3. Students should watch all the videos of the course to learn the course in-depth and entirety.
4. Students should solve weekly assignments that are to be submitted online within the prescribed deadline.
5. Students should register and appear for the course certification exam on scheduled date and time.
6. Students should submit the certificate of course completion to the Faculty Supervisor.
7. Faculty Supervisor shall monitor students' participation and progress at every stage — from course enrolment to certification.

Useful Learning Links:

1. https://swayam.gov.in
2. https://www.nptel.ac.in
3. https://www.coursera.org

Term Work (25 Marks):

Term Work shall be conducted for Total 25 Marks based on the following rubrics:

Performance Level	**Not Qualifying**	**Poor**	**Acceptable**	**Good**	**Excellent**
Marks	00	08	12	16	20
Compliance Status	Not Enrolled for any Course or Not Completed Course	Completed Course, Not Attempted Certification but Completed all Assignments.	Obtained Passing Grade or 40% of Total Score in Certification Exam	Obtained First Class Grades or 60% of Total Score	Obtained Elite Grade or 75% of Total Score

			OR Completed all Assignments with Score Above 70%.		